

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
1 July 2004 (01.07.2004)

PCT

(10) International Publication Number
WO 2004/055670 A3

(51) International Patent Classification⁷: **G06F 9/445**,
15/177

(21) International Application Number:
PCT/IB2003/006048

(22) International Filing Date:
17 December 2003 (17.12.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/434,822 18 December 2002 (18.12.2002) US

(71) Applicant (for all designated States except US): **KONINKLIJKE PHILIPS ELECTRONICS N.V.** [NL/NL];
Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(71) Applicant (for AE only): **U.S. PHILIPS CORPORATION** [US/US]; 1251 Avenue of the Americas, New York,
NY 10510-8001 (US).

(72) Inventor; and

(75) Inventor/Applicant (for US only): **OMATHUNA, Padraig** [IE/US]; 1109 McKay Drive, M/S-41SJ, San
Jose, CA 95131 (US).

(74) Common Representative: **KONINKLIJKE PHILIPS ELECTRONICS N.V.**; c/o LESTER, Shannon, 1109
McKay Drive, M/S-41SJ, San Jose, CA 95131 (US).

(81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

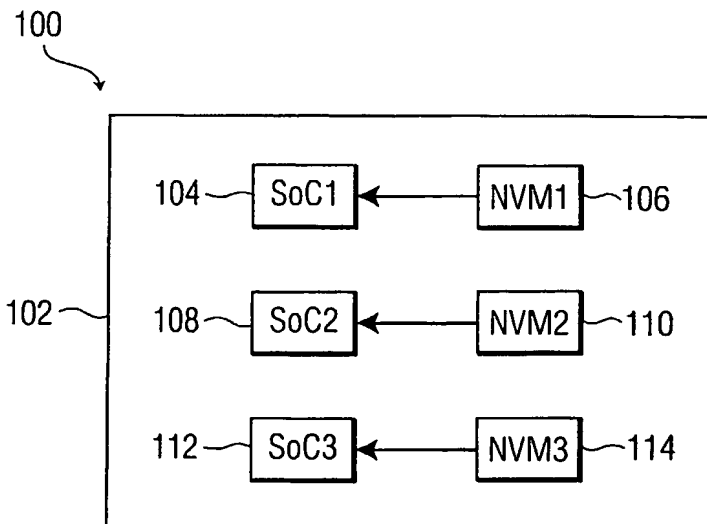
(84) Designated States (*regional*): ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:

— as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW, ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK,

[Continued on next page]

(54) Title: CODE DOWNLOAD IN A SYSTEM HAVING MULTIPLE INTEGRATED CIRCUITS WITH JTAG CAPABILITY



(57) Abstract: An electronic product (500) including a first integrated circuit (502) coupled to a first memory (506) and at least a second integrated circuit (508, 512) coupled (516, 518, 520) to the first integrated circuit. The first integrated circuit loads information, such as a first code image, from the first memory into the first integrated circuit, and executes at least a portion of the first code image. In response to such code execution, the first integrated circuit reads information, such as a second code image, from the first memory and transmits that information to the second integrated circuit. The interface between the first and second integrated circuits for transmission of the information may be a test circuitry (522, 528, 526, 524) interface such as JTAG circuitry. In one embodiment program code is transferred from a single external memory through a first integrated circuit to one or more downstream integrated circuits by way of serially connected JTAG data and control pins.

WO 2004/055670 A3



EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO,
SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA,
GN, GQ, GW, ML, MR, NE, SN, TD, TG)

(88) Date of publication of the international search report:
29 December 2004

Published:

- with international search report
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

A. CLASSIFICATION OF SUBJECT MATTER
 IPC 7 G06F9/445 G06F15/177

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
 IPC 7 G06F H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the International search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 757 639 A (YAMADA MASANORI) 26 May 1998 (1998-05-26) figures 1,6,7 column 1, line 34 - line 40 column 2, line 23 - line 40 column 2, line 61 - column 3, line 4 column 3, line 39 - line 46 column 4, line 39 - line 42	1-18
A	US 5 760 607 A (LEEDS KENNETH E ET AL) 2 June 1998 (1998-06-02) column 1, line 35 - line 40; figure 2	1-18
A	US 6 204 687 B1 (HUNG LAWRENCE C ET AL) 20 March 2001 (2001-03-20) figure 4	14

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☒ Patent family members are listed in annex.

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Date of the actual completion of the international search

18 October 2004

Date of mailing of the international search report

28/10/2004

Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2
 NL - 2280 HV Rijswijk
 Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
 Fax: (+31-70) 340-3016

Authorized officer

Bosch Vivancos, P

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